# Evaluation of the Thermal Performance of a Light Emitting Diode (LED) Package Manufactured using POL-kW Packaging Technology

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## Background

- Power Overlay (POL) Technology
  - Utilizes flexible polyimide substrate & direct metal interconnects to eliminate wire-bonds and solder interfaces
  - Currently used in high density power devices & modules, RF modules, application specific ICS (ASICs), & sensing devices [1,2]
- POL for LED packages
  - Direct bonding of LED dies to polyimide substrate with use of adhesive
  - Thermal vias used to provide efficient thermal path from die to contact pad

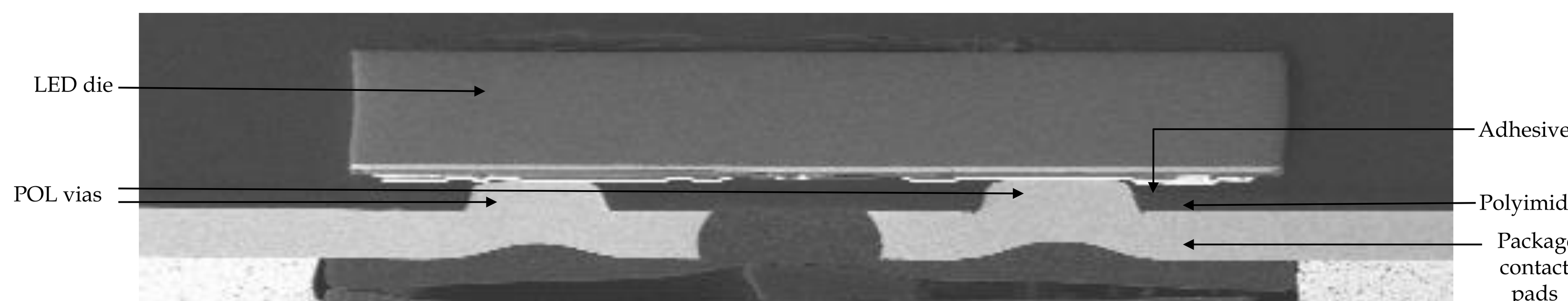


Figure 1: SEM image of the cross-section of the LED prototype manufactured using POL – kw packaging technology

## Objectives

- Evaluate and optimize the use of POL-kw packaging technology for high power LED applications
  - Study effect of geometry parameters & substrate material on LED prototype
  - Estimate PCB level thermal performance of LED prototype using FEA
  - Experimentally validate simulation model using infrared tomography

## Methodology

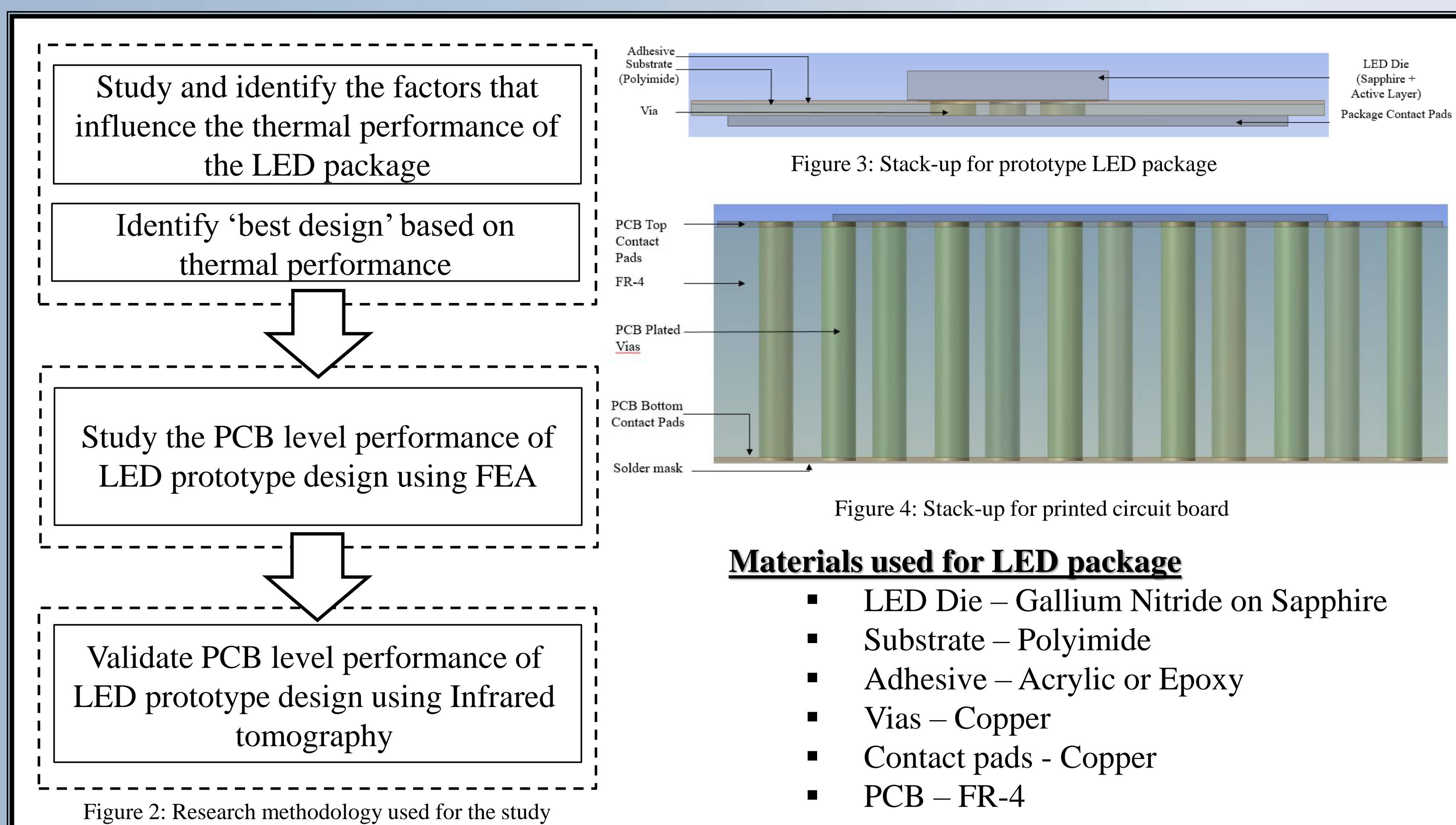


Figure 2: Research methodology used for the study

Figure 3: Stack-up for prototype LED package

Figure 4: Stack-up for printed circuit board

**Materials used for LED package**

- LED Die – Gallium Nitride on Sapphire
- Substrate – Polyimide
- Adhesive – Acrylic or Epoxy
- Vias – Copper
- Contact pads - Copper
- PCB – FR-4

## Results

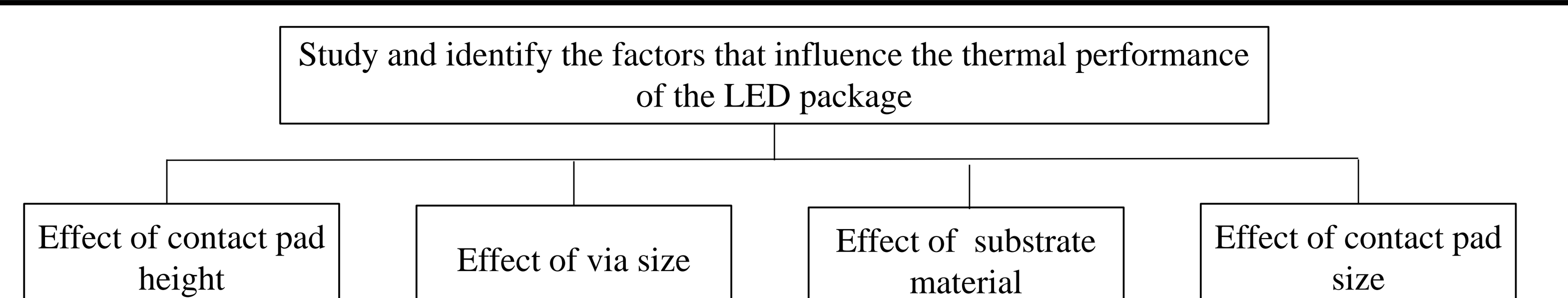


Figure 5: Factors studied for the LED prototype design

| Factor | Factor levels | |
|---|---|---|
| | + | - |
| Contact pad height | 100 µm | 50 µm |
| Via size | 0.200-0.250 µm | 0.100-0.150 µm |
| Substrate material | Polyimide (0.12 W/°C) | Aluminum Nitride (180 W/°C) |
| Contact pad size | 1.46 x 3.07 mm | 1 x 1.5 mm |

Figure 6: Table for factor name and factor levels of the LED prototype design studied

**Analysis of Variance**

| Source | DF | Adj SS | Adj MS | F-Value | P-Value |
|---|---|---|---|---|---|
| Model | 10 | 739.304 | 73.930 | 40642.03 | 0.000 |
| Linear | 4 | 729.722 | 182.430 | 100288.20 | 0.000 |
| Contact pad height | 1 | 1.289 | 1.289 | 708.49 | 0.000 |
| Via size | 1 | 701.707 | 701.707 | 385751.92 | 0.000 |
| Subtrate material | 1 | 26.726 | 26.726 | 14692.36 | 0.000 |
| Contact pad size | 1 | 0.000 | 0.000 | 0.01 | 0.916 |
| 2-Way Interactions | 6 | 9.582 | 1.597 | 877.93 | 0.000 |
| Contact pad height*Via size | 1 | 0.034 | 0.034 | 18.76 | 0.007 |
| Contact pad height*Subtrate material | 1 | 0.060 | 0.060 | 32.93 | 0.002 |
| Contact pad height*Contact pad size | 1 | 0.000 | 0.000 | 0.00 | 0.996 |
| Via size*Subtrate material | 1 | 9.488 | 9.488 | 5215.84 | 0.000 |
| Via size*Contact pad size | 1 | 0.000 | 0.000 | 0.02 | 0.907 |
| Subtrate material*Contact pad size | 1 | 0.000 | 0.000 | 0.02 | 0.907 |
| Error | 5 | 0.009 | 0.002 | | |
| Total | 15 | 739.313 | | | |

Figure 7: ANOVA table for analyzing the significant factors that influence the average surface temperature of the LED prototype

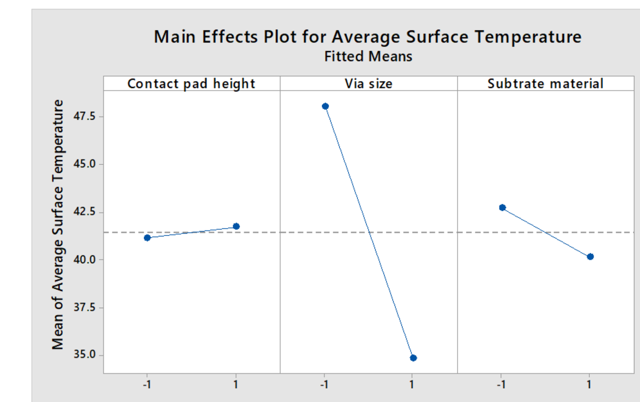


Figure 8: Main effect plot significant factors that influence the average surface temperature of the LED prototype

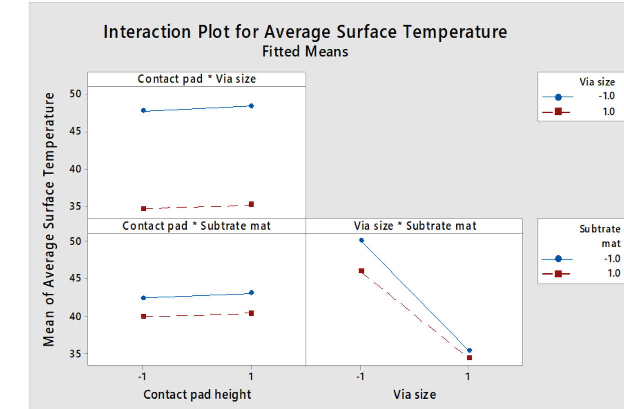


Figure 9: Interaction effect plot significant factors that influence the average surface temperature of the LED prototype

- The contact pad height, via size, & substrate material are the most significant factors that affect the thermal performance of the LED prototype

## Results (FEA Analysis)

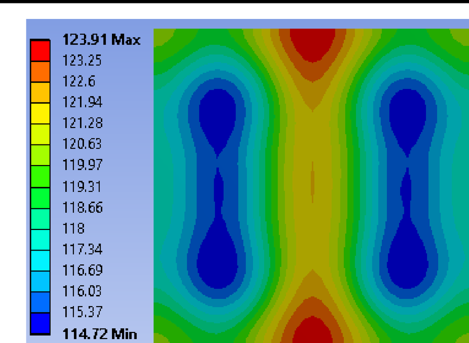


Figure 10: Temperature map of the top surface of the sapphire layer on LED die at input current of 1A

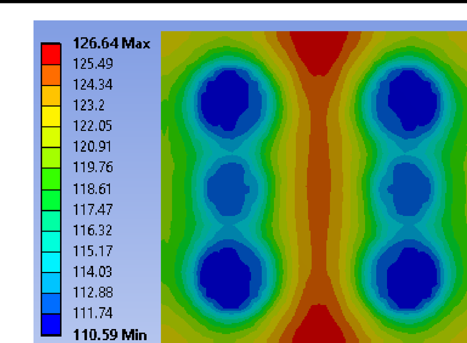


Figure 11: Temperature map of the top surface of the active layer (GaN) in LED die at input current of 1A

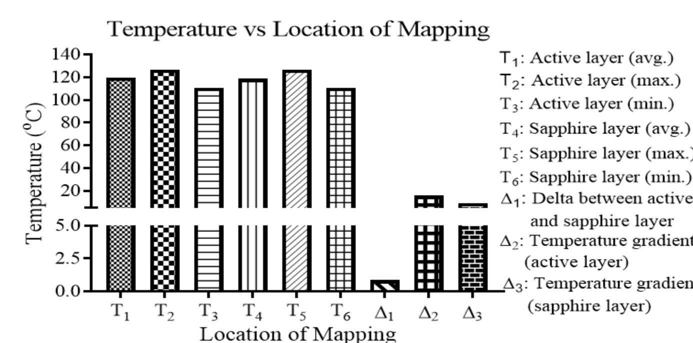


Figure 12: Temperature of active layer (GaN) & sapphire layer at input currents of 1A

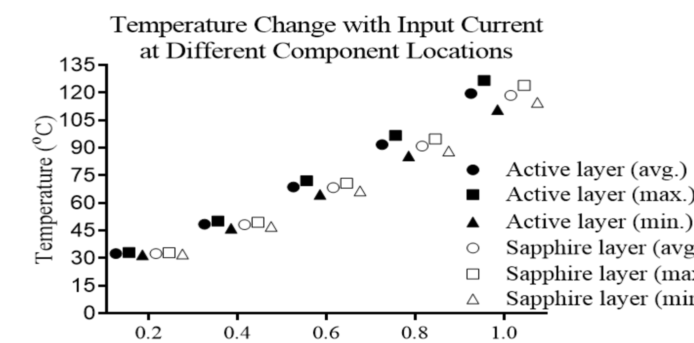


Figure 13: Temperature of active layer (GaN) & sapphire layer at different input currents

## Results (Experimentally Measured)

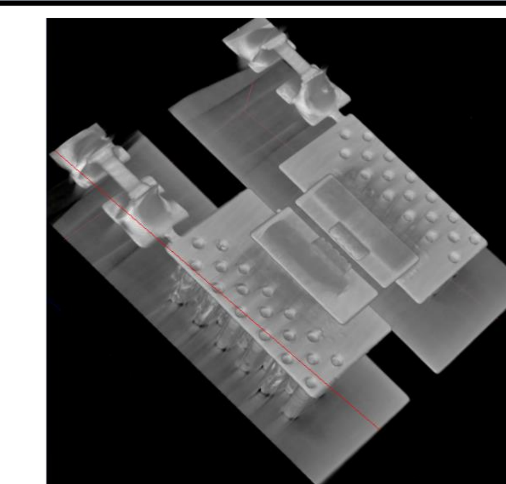

Figure 14: X-Ray image of the POL LED prototype assembled on a PCB

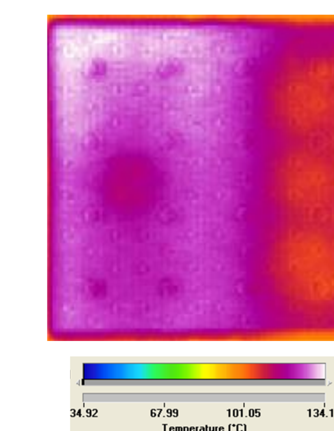


Figure 15: Temperature map of the surface of the LED die at input current of 1A

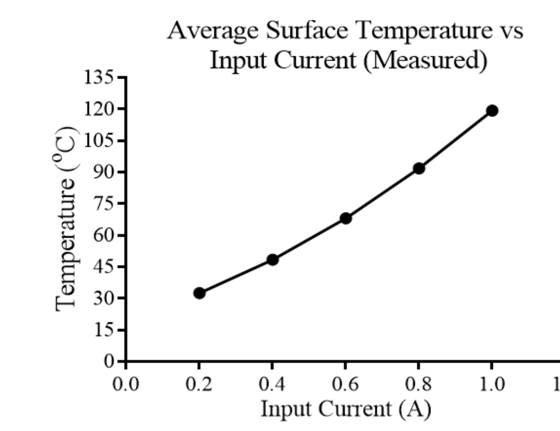


Figure 16: Surface temperature LED die at different input currents

## Conclusions

- Efficient thermal architecture is key to effective thermal management
- Low thermal conductivity of polyimide substrate is the most significant bottleneck in effective thermal management in flexible LED packages
- Increase in size of vias & reduction in contact pad height reduced average temperature of LED prototype
- Increase in size of contact pad did not provide any additional heat spreading benefits
- Temperatures estimated by FEA are validated by temperature measurements using infrared tomography & are in agreement with the FEA model based on average chip temperatures
- Experimental results show slightly higher temperature on cathode side of LED die

## Acknowledgements

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## References

[1] A. Gowda, S. Chauhan, P. McConnelee, K. Chris and Y. Lee, "Power Overlay Packaging Platform for High Performance Electronics," *Chip Scale Review*, pp. 22-27, 19 September 2012

[2] B. Ozmat, C. S. Korman and R. Fillion, "An advanced approach to power module packaging," in *International Workshop on Integrated Power Packaging*, Waltham, 2000